AMENDMENTS TO CLAIMS

Claims 17, 18 and 20-25 are being amended, claims 10-12 and 14-16 are being canceled, and new claims 27-29 are being added. All pending claims are reproduced below.

1.-16. (Canceled)

17. (Currently Amended) A laser driver for driving a laser diode of an optical storage device that includes an optical disk, the laser driver including:

timers that are used to produce mark-space edges on a surface of the optical disk;

driver registers including land and groove amplitude registers;

driver timing memory that stores delays of said timers for various mark-space sequences;

a laser driver serial controller to control serial transfers between said driver registers and driver timing memory of the laser driver and a host, said laser driver serial controller configured to receive a serial enable (SEN) signal, a serial clock (SCLK) signal and a serial data input signal from the host, and said laser driver serial controller configured to send a serial data output signal to the host;

an address shift register to serially receive address bits from ~~a~~ the host, the address bits identifying a location, within said driver registers or said driver timing memory, to which to write data bits, or from which to read data bits;

a data shift register, to serially receive data ~~bit~~ bits from the host during a write operation, and to serially transfer data bits to the host during a read operation[[,]];

an address holding register to receive a parallel transfer of address bits from ~~the~~ said address shift register; and

a data holding register, to receive a parallel transfer of data bits from ~~the~~ said data shift register during a write operation, and to transfer in parallel data bits to ~~the~~ said data shift register during a read operation;

wherein during a write operation, after the parallel transfers of the address bits and data bits from said address and data shift registers to said address and data holding registers, said address and data shift registers are available to serially receive additional address bits and data bits from the host, prior to the data bits in said data holding register being written to the location within said driver registers or said driver timing memory identified by the address in said address holding register ~~read operation, data bits transferred from the data holding register to the host, are associated with a previous read operation~~.

18. (Currently Amended) The ~~system~~ laser driver of claim 17, wherein use of said data holding register and said address holding register, during serial transfers between said laser driver serial controller and the host, enables said laser driver serial controller to operate at a higher frequency than other components of said laser driver, thus allowing for serial transfer speeds that exceed operating speeds of other components of said laser driver ~~write operation, after the parallel transfers of the address bits and data bits from the address and data shift registers to the address and data holding registers, the address and data shift registers are available to serially receive additional address bits and data bits from the host~~.

19. (Canceled)

20. (Currently Amended) The laser driver of claim 17, wherein ~~the~~ said laser driver serial controller includes a counter that receives ~~a~~ the serial clock (SCLK) signal, and wherein ~~the~~ said laser driver serial controller uses ~~the~~ said counter to determine which bits are address bits and which bits are data bits.

21. (Currently Amended) The laser driver of claim 20, wherein, during a write operation, ~~the~~ said laser driver serial controller includes a switch to select between transferring bits to ~~the~~ said address shift register and ~~the~~ said data shift register.

22. (Currently Amended) The laser driver of claim 17, further comprising:

a parallel address bus connecting ~~the~~ said address holding register to ~~a plurality of~~ said driver registers and said driver timing memory; and

a parallel data bus connecting ~~the~~ said data holding register to ~~the plurality of~~ said driver registers and said driver timing memory.

23. (Currently Amended) The laser driver of claim 17, wherein during a read operation, data bits transferred from said data shift register to the host, are associated with a previous read operation ~~further comprising:~~

~~a parallel address bus connecting the address holding register to a timing memory; and~~

~~a parallel data bus connecting the data holding register to the timing memory~~.

24. (Currently Amended) The laser driver of claim 17, wherein ~~the~~ said address and data holding registers each comprises a latch.

25. (Currently Amended) A laser driver, including:

a serial controller to control serial transfers between the laser driver and a host wherein the serial controller includes a counter that receives a serial clock (SCLK) signal, and wherein the serial controller uses ~~the~~ a counter to determine which bits are address bits and which bits are data bits;

an address shift register to serially receive address bits from a host, the address bits identifying a location to which to write data bits, or from which to read data bits;

a data shift register, to serially receive data ~~bit~~ bits from the host during a write operation, and to serially transfer data bits to the host during a read operation;

an address holding register to receive a parallel transfer of address bits from the address shift register;

a data holding register, to receive a parallel transfer of data bits from the data shift register during a write operation, and to transfer in parallel data bits to the data shift register during a read operation; and

logic that receives at least two least significant bits from the counter to thereby provide a level of confidence that a serial enable signal going high was not due to a glitch.

26. (Original) The laser driver of claim 25, wherein the logic includes:

an AND gate that receives the at least two least significant bits from the counter;

a 1-bit latch that includes a data input that receives an output from the AND gate, and an enable input attached to a send enable (SEN) line; and

a strobe circuit including an enable input that receives an output of the 1-bit latch;

wherein an output of the strobe circuit is used to ensure that possible glitches on the SEN line do not cause accidental reads or writes.

27 (New) The laser driver of claim 23, wherein during a read operation, requested data bits will be transferred, serially, from said data shift register to the host the next time the host performs a read operation.

28. (New) The laser driver of claim 23, wherein during a read operation, N+1 read cycles are required to read N addresses.

29. (New) The laser driver of claim 27, wherein the $N+1^{th}$ read cycle is a dummy read cycle that is used to transfer data bits associated with an N^{th} address, from said data shift register to the host.